

CLAIMS

1 1. (Original) A data processor for use in a wireless communication device,
2 comprising:
3 a processing unit;
4 an instruction pipeline circuit;
5 at least one processing module;
6 a timer for generating a time-out interval; and
7 power control logic for detecting a sleep instruction and placing the processing unit,
8 instruction pipeline circuit and at least one processing module in a low-power state, where the
9 power control logic is operative in response to a wake-up signal to reactivate the instruction
10 pipeline circuit, and consequently at least one processing module only to the extent required by
11 the wake-up signal.

1 2. (Original) The processor of claim 1, where the instruction pipeline circuit
2 comprises a multi-stage instruction pipeline circuit.

1 3. (Original) The processor of claim 1, where the wake-up signal comprises a
2 logical OR combination of one or more predetermined wake-up conditions and the time-out
3 interval.

1 4. (Original) The processor of claim 1, where the power control logic comprises
2 instruction decode logic to detect the sleep instruction.

1 5. (Original) The processor of claim 1, where the power control logic comprises
2 branch condition logic to respond to the wake-up signal.

1 6. (Original) The processor of claim 1, where the power control logic, having
2 specified one or more wake-up conditions that the processing unit will respond to when in a low-
3 power state, generates the wake-up signal upon detecting the one or more wake-up conditions or
4 the time-out interval.

1 7. (Original) The processor of claim 1, where the power control logic instructs
2 the instruction pipeline circuit to complete any instructions preceding the sleep instruction.

1 8. (Original) The processor of claim 7, where the power control logic instructs
2 the instruction pipeline circuit to cease fetching new instructions after encountering a sleep
3 instruction whose wake-up conditions are currently deasserted.

1 9. (Original) The processor of claim 1, wherein the processing unit, instruction
2 pipeline circuit and at least one processing module are formed together on a common silicon
3 substrate using CMOS processing.

1 10. (Original) The processor of claim 6, wherein the wake-up conditions and
2 time-out interval are stored in a register by the power control logic.

3 11. (Original) An article of manufacture having at least one recordable medium
4 having stored thereon executable instructions and data which, when executed by at least one
5 processing device, cause the at least one processing device to:

6 detect a sleep instruction for the processing device;
7 specify one or more wake-up conditions and a time-out interval;
8 power down an instruction pipeline and one or more processor modules;
9 reactivate the instruction pipeline upon detection of a wake-up signal corresponding to
10 either a wake-up condition or the time-out interval, and
11 process one or more instructions in the instruction pipeline to reactivate any of the one or
12 more processor modules required to respond to a detected wake-up condition.

1 12. (Original) The article of manufacture of claim 11, wherein the processing
2 device executes any instructions received by the instruction pipeline before the sleep instruction
3 is received.

1 13. (Original) The article of manufacture of claim 11, wherein the instruction
2 pipeline comprises a multistage instruction pipeline, and the processing device reactivates only

3 stages in the multistage instruction pipeline and/or the function units needed to process one or
4 more instructions necessary to analyze and respond to the wake-up signal.

1 14. (Original) The article of manufacture of claim 11, further comprising a
2 register for holding the specified wake-up conditions and time out signal.

1 15. (Original) The article of manufacture of claim 11, where the processing
2 device is implemented as part of a single-chip wireless communication device.

1 16. (Original) The article of manufacture of claim 11, where the executable
2 instructions and data comprise control logic for controlling the operation of the processing
3 device.

1 17. (Original) The article of manufacture of claim 11, where the processing
2 device powers down the one or more processor modules by freezing a clock signal for said one
3 or more modules.

1 18. (Original) The article of manufacture of claim 11, where the processing
2 device powers down the one or more processor modules by placing said one or more modules in
3 an idle mode.

1 19. (Original) A method for managing power in a communications processor by
2 selectively removing one or more processor modules from a standby mode, comprising:
3 storing one or more wake-up conditions and a time-out interval in a register;
4 receiving a processor sleep instruction;
5 executing any pending instructions received by the processor before the sleep instruction;
6 powering down the one or more processor modules;
7 receiving a processor wake-up signal corresponding to one of said wake-up conditions or
8 said time-out interval;
9 powering up only the processor modules required to respond to the detected processor
10 wake-up signal.

1 20. (Original) The method of claim 19, wherein one of the processor modules
2 comprises an instruction pipeline circuit.